AP5151 ADVANCED DIGITAL SYSTEM DESIGN L T P C
3 0 0 3

OBJECTIVES:

- To introduce methods to analyze and design synchronous and asynchronous sequential circuits
- To introduce the architectures of programmable devices
- To introduce design and implementation of digital circuits using programming tools

UNIT I SEQUENTIAL CIRCUIT DESIGN 9

Analysis of clocked synchronous sequential circuits and modeling- State diagram, state table, state table assignment and reduction-Design of synchronous sequential circuits design of iterative circuits-ASM chart and realization using ASM

UNIT II ASYNCHRONOUS SEQUENTIAL CIRCUIT DESIGN 9

Analysis of asynchronous sequential circuit – flow table reduction-races-state assignment-transition table and problems in transition table- design of asynchronous sequential circuit-Static, dynamic and essential hazards – data synchronizers – mixed operating mode asynchronous circuits – designing vending machine controller

UNIT III FAULT DIAGNOSIS AND TESTABILITY ALGORITHMS 9

Fault table method-path sensitization method – Boolean difference method-D algorithm - Tolerance techniques – The compact algorithm – Fault in PLA – Test generation-DFT schemes – Built in self test

UNIT IV SYNCHRONOUS DESIGN USING PROGRAMMABLE DEVICES 9

Programming logic device families – Designing a synchronous sequential circuit using PLA/PAL – Realization of finite state machine using PLD – FPGA – Xilinx FPGA-Xilinx 4000

UNIT V SYSTEM DESIGN USING VERILOG 9

Hardware Modelling with Verilog HDL – Logic System, Data Types and Operators For Modelling in Verilog HDL - Behavioural Descriptions in Verilog HDL – HDL Based Synthesis – Synthesis of Finite State Machines– structural modeling – compilation and simulation of Verilog code –Test bench - Realization of combinational and sequential circuits using Verilog – Registers – counters – sequential machine – serial adder – Multiplier- Divider – Design of simple microprocessor

TOTAL : 45 PERIODS

OUTCOMES:

At the end of the course, the student should be able to:

- Analyze and design sequential digital circuits
- Identify the requirements and specifications of the system required for a given application
- Design and use programming tools for implementing digital circuits of industry standards

REFERENCES:

1. Charles H.Roth Jr “Fundamentals of Logic Design” Thomson Learning 2004
2. M.D.Ciletti , Modeling, Synthesis and Rapid Prototyping with the Verilog HDL, Prentice Hall, 1999
3. M.G.Arnold, Verilog Digital – Computer Design, Prentice Hall (PTR), 1999.
4. Nripendra N Biswas “Logic Design Theory” Prentice Hall of India,2001
5. Parag K.Lala “Fault Tolerant and Fault Testable Hardware Design” B S
6. Publications,2002
7. Parag K.Lala “Digital system Design using PLD” B S Publications,2003
8. S. Palnitkar , Verilog HDL – A Guide to Digital Design and Synthesis, Pearson , 2003.

VL5101 **CMOS DIGITAL VLSI DESIGN** **L T P C**
3 0 0 3

OBJECTIVES:

- This course deals comprehensively with all aspects of transistor level design of all the digital building blocks common to all CMOS microprocessors, DPSs, network processors, digital backend of all wireless systems etc.
- The focus will be on the transistor level design and will address all important issues related to size, speed and power consumption. The units are classified according to the important building and will introduce the principles and design methodology in terms of the dominant circuit choices, constraints and performance measures.

UNIT I MOS TRANSISTOR PRINCIPLES AND CMOS INVERTER 12

MOS(FET) Transistor Characteristic under Static and Dynamic Conditions, MOS Transistor Secondary Effects, Process Variations, Technology Scaling, Internet Parameter and electrical wise models CMOS Inverter - Static Characteristic, Dynamic Characteristic, Power, Energy, and Energy Delay parameters.

UNIT II COMBINATIONAL LOGIC CIRCUITS 9

Propagation Delays, Stick diagram, Layout diagrams, Examples of combinational logic design, Elmore's constant, Dynamic Logic Gates, Pass Transistor Logic, Power Dissipation, Low Power Design principles.

UNIT III SEQUENTIAL LOGIC CIRCUITS 9

Static Latches and Registers, Dynamic Latches and Registers, Timing Issues, Pipelines, Pulse and sense amplifier based Registers, Nonbistable Sequential Circuits.

UNIT IV ARITHMETIC BUILDING BLOCKS AND MEMORY ARCHITECTURES 9

Data path circuits, Architectures for Adders, Accumulators, Multipliers, Barrel Shifters, Speed and Area Tradeoffs, Memory Architectures, and Memory control circuits.

UNIT V INTERCONNECT AND CLOCKING STRATEGIES 6

Interconnect Parameters – Capacitance, Resistance, and Inductance, Electrical Wire Models, Timing classification of Digital Systems, Synchronous Design, Self-Timed Circuit Design.

TOTAL: 45 PERIODS

OUTCOMES:

At the end of the course, the student should be able to:

- Carry out transistor level design of the most important building blocks used in digital CMOS VLSI circuits.
- Discuss design methodology of arithmetic building block
- Analyze tradeoffs of the various circuit choices for each of the building block.

REFERENCES:

1. Jan Rabaey, Anantha Chandrakasan, B Nikolic, "Digital Integrated Circuits: A Design Perspective". Second Edition, Feb 2003, Prentice Hall of India.
2. Jacob Baker "CMOS: Circuit Design, Layout, and Simulation, Third Edition", Wiley IEEE Press 2010 3rd Edition.
3. M J Smith, "Application Specific Integrated Circuits", Addisson Wesley, 1997
4. N.Weste, K. Eshraghian, " Principles of CMOS VLSI Design". Second Edition, 1993 Addision Wesley.

VL5191 **DSP INTEGRATED CIRCUITS** **L T P C**
3 0 0 3

OBJECTIVES:

- To familiarize the concept of DSP and DSP algorithms.
- Introduction to Multirate systems and finite wordlength effects
- To know about the basic DSP processor architectures and the synthesis of the processing elements

UNIT I INTRODUCTION TO DSP INTEGRATED CIRCUITS 9

Introduction to Digital signal processing, Sampling of analog signals, Selection of sample frequency, Signal- processing systems, Frequency response, Transfer functions, Signal flow graphs, Filter structures, Adaptive DSP algorithms, DFT-The Discrete Fourier Transform, FFT Algorithm, Image coding, Discrete cosine transforms, Standard digital signal processors, Application specific ICs for DSP, DSP systems, DSP system design, Integrated circuit design.

UNIT II DIGITAL FILTERS AND FINITE WORD LENGTH EFFECTS 9

FIR filters, FIR filter structures, FIR chips, IIR filters, Specifications of IIR filters, Mapping of analog transfer functions, Mapping of analog filter structures, Multi rate systems, Interpolation with an integer factor L, Sampling rate change with a ratio L/M, Multi rate filters. Finite word length effects - Parasitic oscillations, Scaling of signal levels, Round-off noise, Measuring round-off noise, Coefficient sensitivity, Sensitivity and noise.

UNIT III DSP ARCHITECTURES 9

DSP system architectures, Standard DSP architecture-Harvard and Modified Harvard architecture. Ideal DSP architectures, Multiprocessors and multi computers, Systolic and Wave front arrays, Shared memory architectures.

UNIT IV SYNTHESIS OF DSP ARCHITECTURES 9

Synthesis: Mapping of DSP algorithms onto hardware, Implementation based on complex PEs, Shared memory architecture with Bit – serial PEs. Combinational & sequential networks- Storage elements – clocking of synchronous systems, Asynchronous systems -FSM

UNIT V ARITHMETIC UNIT AND PROCESSING ELEMENTS 9

Conventional number system, Redundant Number system, Residue Number System, Bit-parallel and Bit-Serial arithmetic, Digit Serial arithmetic, CORDIC Algorithm, Basic shift accumulator, Reducing the memory size, Complex multipliers, Improved shift-accumulator. Case Study: DCT and FFT processor

TOTAL: 45 PERIODS

OUTCOMES:

- Get to know about the Digital Signal Processing concepts and its algorithms
- Get an idea about finite word length effects in digital filters
- Concept behind multi rate systems is understood.
- Get familiar with the DSP processor architectures and how to perform synthesis of processing elements

REFERENCES:

1. B.Venkatramani, M.Bhaskar, “Digital Signal Processors”, Tata McGraw-Hill, 2002.
2. John J. Proakis, Dimitris G. Manolakis, “Digital Signal Processing”, Pearson Education, 2002.
3. Keshab Parhi, “VLSI Digital Signal Processing Systems design & Implementation”, John Wiley & Sons, 1999.
4. Lars Wanhammer, “DSP Integrated Circuits”, Academic press, New York, 1999.

VL5102	CAD FOR VLSI CIRCUITS	L T P C
		3 0 0 3

OBJECTIVES:

The students should be made to:

- Learn VLSI Design methodologies
- Understand VLSI design automation tools
- Study modelling and simulation

UNIT I INTRODUCTION TO VLSI DESIGN FLOW 9

Introduction to VLSI Design methodologies, Basics of VLSI design automation tools, Algorithmic Graph Theory and Computational Complexity, Tractable and Intractable problems, General purpose methods for combinatorial optimization.

UNIT II LAYOUT, PLACEMENT AND PARTITIONING 9

Layout Compaction, Design rules, Problem formulation, Algorithms for constraint graph compaction, Placement and partitioning, Circuit representation, Placement algorithms, Partitioning

UNIT III FLOOR PLANNING AND ROUTING 9

Floor planning concepts, Shape functions and floorplan sizing, Types of local routing problems, Area routing, Channel routing, Global routing, Algorithms for global routing.

UNIT IV SIMULATION AND LOGIC SYNTHESIS 9

Simulation, Gate-level modeling and simulation, Switch-level modeling and simulation, Combinational Logic Synthesis, Binary Decision Diagrams, Two Level Logic Synthesis.

UNIT V HIGH LEVEL SYNTHESIS 9

Hardware models for high level synthesis, internal representation, allocation, assignment and scheduling, scheduling algorithms, Assignment problem, High level transformations.

TOTAL: 45 PERIODS

OUTCOMES:

At the end of this course, the students should be able to:

- Outline floor planning and routing
- Explain Simulation and Logic Synthesis
- Discuss the hardware models for high level synthesis

REFERENCES:

1. N.A. Sherwani, "Algorithms for VLSI Physical Design Automation", Kluwer Academic Publishers, 2002.
2. S.H. Gerez, "Algorithms for VLSI Design Automation", John Wiley & Sons, 2002.
3. Sadiq M. Sait, Habib Youssef, “VLSI Physical Design automation: Theory and Practice”, World Scientific 1999.
4. Steven M.Rubin, “Computer Aids for VLSI Design”, Addison Wesley Publishing 1987.

VL5103 **ANALOG IC DESIGN** **L T P C**
4 0 0 4

OBJECTIVES

- To study MOS devices modelling and scaling effects.
- To familiarize the design of single stage and multistage MOS amplifier and analysis their frequency responses.
- To study the different design parameters in designing voltage reference and OPAMP circuits.

UNIT I MOSFET METRICS **12**

Simple long channel MOSFET theory – SPICE Models – Technology trend, Need for Analog design - Sub-micron transistor theory, Short channel effects, Narrow width effect, Drain induced barrier lowering, Sub-threshold conduction, Reliability, Digital metrics, Analog metrics, Small signal parameters, Unity Gain Frequency, Miller's approximation

UNIT II SINGLE STAGE AND TWO STAGE AMPLIFIERS **12**

Single Stage Amplifiers – Common source amplifier with resistive load, diode load, constant current load, Source degeneration Source follower, Input and output impedance, Common gate amplifier - Differential Amplifiers – differential and common mode response, Input swing, gain, diode load and constant current load - Basic Two Stage Amplifier, Cut-off frequency, poles and zeros

UNIT III FREQUENCY RESPONSE OF SINGLE STAGE AND TWO STAGE AMPLIFIERS **12**

Frequency Response of Single Stage Amplifiers – Noise in Single stage Amplifiers – Stability and Frequency Compensation in Single stage Amplifiers, Frequency Response of Two Stage Amplifiers, – Noise in two stage Amplifiers – Stability, gain and phase margins, Frequency Compensation in two stage Amplifiers, Effect of loading in feedback networks,

UNIT IV CURRENT MIRRORS AND REFERENCE CIRCUITS **12**

Cascode, Negative feedback, Wilson, Regulated cascode, Bandgap voltage reference, Constant Gm biasing, supply and temperature independent reference, curvature compensation, trimming, Effect of transistor mismatch in analog design

UNIT V OP AMPS **12**

Gilbert cell and applications, Basic two stage OPAMP, two-pole system response, common mode and differential gain, Frequency response of OPAMP, CMFB circuits, slew rate, power supply rejection ratio, random offset, systematic offset, Noise, Output stage, OTA and OPAMP circuits - Low voltage OPAMP

TOTAL : 60 PERIODS

OUTCOMES:

- To design MOS single stage, multistage amplifiers and OPAMP for desired frequencies
- Analyze Stability, frequency response, and Noise in MOS amplifiers

REFERENCES:

1. Behzad Razavi, "Design of Analog CMOS Integrated Circuits", McGraw Hill, 2000
2. Philip E.Allen, "CMOS Analog Circuit Design", Oxford University Press, 2013
3. Paul R.Gray, "Analysis and Design of Analog Integrated Circuits", Wiley Student edition, 5th edition, 2009.
4. R.Jacob Baker, "CMOS: Circuit Design, Layout , and Simulation", Wiley Student Edition, 2009

VL5111 **VLSI DESIGN LABORATORY I** **L T P C**
0 0 4 2

OBJECTIVES:

The laboratory based study for the entire program is clubbed under three categories. One is the FPGA based design methodology; the second is the simulation of analog building blocks, and analog and digital CAD design flow. Experiments pertaining to the former two topics are covered in this lab course and those pertaining to the latter will be covered in VLSI Design Lab II.

FPGAs are important platform used throughout the industry both in their own right in building complete systems. They are also used as validation/verification platforms prior to undertaking cost and time intensive design and fabrication of custom VLSI designs. Starting from high level design entry in the form VHDL/Verilog codes, the students will be carrying out complete hardware level FPGA validation of important digital algorithms. In addition, exercises on the SPICE simulation of the basic CMOS analog building blocks will be carried out.

EXPERIMENTS:

1. Understanding Synthesis principles. Back annotation.
2. Test vector generation and timing analysis of sequential and combinational logic design realized using HDL languages.
3. FPGA real time programming and I/O interfacing.
4. Interfacing with Memory modules in FPGA Boards.
5. Verification of design functionality implemented in FPGA by capturing the signal in DSO.
6. Real time application development.
7. Design Entry Using VHDL or Verilog examples for Digital circuit descriptions using HDL languages sequential, concurrent statements and structural description.

TOTAL : 60 PERIODS

OUTCOMES:

At the end of the course, the student should be able to: After completing this course, given a digital system specification, the student should be able to map it onto FPGA paltform and carry out a series of validations design starting from design entry to hardware testing. In addition, the student also will be able to design and carry out time domain and frequency domain simulations of simple analog building blocks, study the pole zero behaviors of feedback based circuits and compute the input/output impedances.

VL5201 **TESTING OF VLSI CIRCUITS** **L T P C**
3 0 0 3

OBJECTIVES :

The students should be made to:

- Understand logic fault models
- Learn test generation for sequential and combinational logic circuits

UNIT I TESTING AND FAULT MODELLING **9**

Introduction to testing – Faults in Digital Circuits – Modelling of faults – Logical Fault Models –Fault detection – Fault Location – Fault dominance – Logic simulation – Types of simulation –Delay models – Gate Level Event – driven simulation.

UNIT II TEST GENERATION **9**

Test generation for combinational logic circuits – Testable combinational logic circuit design – Test generation for sequential circuits – design of testable sequential circuits.

UNIT III DESIGN FOR TESTABILITY 9

Design for Testability – Ad-hoc design – generic scan based design – classical scan based design– system level DFT approaches.

UNIT IV SELF – TEST AND TEST ALGORITHMS 9

Built-In self-test – test pattern generation for BIST – Circular BIST – BIST Architectures – Testable Memory Design – Test Algorithms – Test generation for Embedded RAMs.

UNIT V FAULT DIAGNOSIS 9

Logical Level Diagnosis – Diagnosis by UUT reduction – Fault Diagnosis for Combinational Circuits– Self-checking design – System Level Diagnosis.

TOTAL : 45 PERIODS

OUTCOMES:

At the end of this course, the students should be able to:

- Prepare design for testability
- Discuss test algorithms
- Explain fault diagnosis

REFERENCES:

1. A.L.Crouch, “Design Test for Digital IC’s and Embedded Core Systems”, Prentice HallInternational, 2002.
2. M.Abramovici, M.A.Breuer and A.D. Friedman, “Digital systems and Testable Design”, JaicoPublishing House, 2002.
3. M.L.Bushnell and V.D.Agrawal, “Essentials of Electronic Testing for Digital, Memory andMixed-
   Signal VLSI Circuits”, Kluwer Academic Publishers, 2002.
4. P.K. Lala, “Digital Circuit Testing and Testability”, Academic Press, 2002.

VL5291 VLSI SIGNAL PROCESSING L T P C
3 0 0 3

OBJECTIVES:

- To introduce techniques for altering the existing DSP structures to suit VLSI implementations.
- To introduce efficient design of DSP architectures suitable for VLSI

UNIT I PIPELINING AND PARALLEL PROCESSING OF DIGITAL FILTERS 9

Introduction to DSP systems – Typical DSP algorithms, Data flow and Dependence graphs – critical path, Loop bound, iteration bound, Longest path matrix algorithm, Pipelining and Parallel processing of FIR filters, Pipelining and Parallel processing for low power.

UNIT II ALGORITHMIC STRENGTH REDUCTION TECHNIQUE I 9

Retiming – definitions and properties, Unfolding – an algorithm for unfolding, properties of unfolding, sample period reduction and parallel processing application, Algorithmic strength reduction in filters and transforms – 2-parallel FIR filter, 2-parallel fast FIR filter, DCT architecture, rank-order filters, Odd-Even merge-sort architecture, parallel rank-order filters.

UNIT III ALGORITHIMIC STRENGTH REDUCTION -II 9

Fast convolution – Cook-Toom algorithm, modified Cook-Toom algorithm, Pipelined and parallel recursive filters – Look-Ahead pipelining in first-order IIR filters, Look-Ahead pipelining with powerof-2 decomposition, Clustered look-ahead pipelining, Parallel processing of IIR filters, combined pipelining and parallel processing of IIR filters.

UNIT IV BIT-LEVEL ARITHMETIC ARCHITECTURES 9

Bit-level arithmetic architectures – parallel multipliers with sign extension, parallel carry-ripple and carry-save multipliers, Design of Lyon‟s bit-serial multipliers using Horner‟s rule, bit-serial FIR filter, CSD representation, CSD multiplication using Horner‟s rule for precision improvement, Distributed Arithmetic fundamentals and FIR filters

UNIT V NUMERICAL STRENGTH REDUCTION, WAVE AND ASYNCHRONOUS PIPELINING 9

Numerical strength reduction – subexpression elimination, multiple constant multiplication, iterative matching, synchronous pipelining and clocking styles, clock skew in edge-triggered single phase clocking, two-phase clocking, wave pipelining. Asynchronous pipelining bundled data versus dual rail protocol.

TOTAL: 45 PERIODS

OUTCOME:

- Ability to modify the existing or new DSP architectures suitable for VLSI.

REFERENCES:

1. Keshab K. Parhi, “ VLSI Digital Signal Processing Systems, Design and implementation “, Wiley, Interscience, 2007.
2. U. Meyer – Baese, “ Digital Signal Processing with Field Programmable Gate Arrays”, Springer, Second Edition, 2004.

VL5202 LOW POWER VLSI DESIGN L T P C
3 0 0 3

OBJECTIVES:

- Identify sources of power in an IC.
- Identify the power reduction techniques based on technology independent and technology dependent
- Power dissipation mechanism in various MOS logic style.
- Identify suitable techniques to reduce the power dissipation.
- Design memory circuits with low power dissipation.

UNIT I POWER DISSIPATION IN CMOS 9

Physics of power dissipation in CMOS FET devices – Hierarchy of limits of power – Sources of power consumption – Static Power Dissipation, Active Power Dissipation - Designing for Low Power, Circuit Techniques For Leakage Power Reduction - Basic principle of low power design.

UNIT II POWER OPTIMIZATION 9

Logic level power optimization – Circuit level low power design – Standard Adder Cells, CMOS Adders Architectures-BiCMOS adders - Low Voltage Low Power Design Techniques, Current Mode Adders -Types Of Multiplier Architectures, Braun, Booth and Wallace Tree Multipliers and their performance comparison

UNIT III DESIGN OF LOW POWER CMOS CIRCUITS 9

Computer arithmetic techniques for low power system – low voltage low power static Random access and dynamic Random access memories – low power clock, Inter connect and layout design – Advanced techniques – Special techniques.

UNIT IV POWER ESTIMATION **9**

Power Estimation techniques – logic power estimation – Simulation power analysis –Probabilistic power analysis.

UNIT V SYNTHESIS AND SOFTWARE DESIGN FOR LOW POWER **9**

Synthesis for low power – Behavioral level transform – software design for low power.

TOTAL: 45 PERIODS

OUTCOMES:

- The student will get to know the basics and advanced techniques in low power design which is a hot topic in today"s market where the power plays major role.
- The reduction in power dissipation by an IC earns a lot including reduction in size, cost and etc.

REFERENCES:

1. AbdelatifBelaouar, Mohamed.I.Elmasry, "Low power digital VLSI design", Kluwer, 1995.
2. A.P.Chandrasekaran and R.W.Broadersen, "Low power digital CMOS design", Kluwer,1995.
3. DimitriosSoudris, C.Pignet, Costas Goutis,"Designing CMOS Circuits for Low Power"Kluwer, 2002.
4. Gary Yeap, "Practical low power digital VLSI design", Kluwer, 1998.
5. James B.Kulo, Shih-Chia Lin, "Low voltage SOI CMOS VLSI devices and Circuits", John Wiley and sons, inc. 2001.
6. J.B.Kulo and J.H Lou, "Low voltage CMOS VLSI Circuits", Wiley 1999.
7. Kaushik Roy and S.C.Prasad, "Low power CMOS VLSI circuit design", Wiley, 2000.
8. Kiat-send Yeo, Kaushik Roy "Low-Voltage, Low-power VLSI Subsystem", Tata McGraw-Hill, 2009

VL5211 VLSI DESIGN LABORATORY II **L T P C**
0 0 4 2

OBJECTIVE:

The focus of this course the CAD based VLSI design flow. The entire VLSI design industry makes use of this design flow in some for or the other. Proficiency and familiarity with the various stages of a typical 'state of this design flow is a prerequisite for any student who wishes to be apart of either the industry or their search in VLSI over one full semester exposure to various stages of a typical state of the art CAD VLSI tool be provided by various experiments designed to bring out the key aspects of simulation, and power and clock routing modules. ASIC RTL realization of an available open source MCU

EXPERIMENTS :

To synthesize and understand the Boolean optimization in synthesis. Static timing analyses procedures and constraints. Critical path considerations. Scan chain insertion, Floor planning, Routing and Placement procedures. Power planning, Layout generation, LVS and back annotation, Total power estimate. Analog circuit simulation. Simulation of logic gates, Current mirrors, Current sources, Differential amplifier in Spice.

Layout generations, LVS, Back annotation

TOTAL: 60 PERIODS

OUTCOMES:

The student would have hands on experience in the carrying out a complete VLSI based experiments using / CADENCE/ TANNER/ Mentor/Synopsis

OUTCOMES:

- To design and model MOSFET devices, taking into consideration process dependant parameters
- To utilize device level simulators

REFERENCES :

1. Arora, N., “MOSFET Models for VLSI Circuit Simulation”, Springer-Verlag, 1993
2. Chua, L.O. and Lin, P.M., “Computer-Aided Analysis of Electronic Circuits: Algorithms and Computational Techniques”, Prentice-Hall., 1975
3. Fjeldly, T., Yetterdal, T. and Shur, M., “Introduction to Device Modeling and Circuit Simulation”, Wiley-Interscience., 1997
4. Grasser, T., “Advanced Device Modeling and Simulation”, World Scientific Publishing Company., 2003
5. Selberherr, S., “Analysis and Simulation of Semiconductor Devices”, Springer-Verlag., 1984
6. Trond Ytterdal, Yuhua Cheng and Tor A. FjeldlyWayne Wolf, “Device Modeling for Analog and RF CMOS Circuit Design”, John Wiley & Sons Ltd.

AP5292 DIGITAL IMAGE PROCESSING L T P C
3 0 0 3

OBJECTIVES :

The students should be made to:

- Understand fundamentals of digital images
- Learn different image transforms
- Study concept of segmentation

UNIT I DIGITAL IMAGE FUNDAMENTALS 9

A simple image model, Sampling and Quantization, Imaging Geometry, Digital Geometry, Image Acquisition Systems, Different types of digital images. Basic concepts of digital distances, distance transform, medial axis transform, component labeling, thinning, morphological processing, extension to gray scale morphology.

UNIT II IMAGE TRANSFORMS 9

1D DFT, 2D transforms - DFT, DCT, Discrete Sine, Walsh, Hadamard, Slant, Haar, KLT, SVD, Wavelet transform.

UNIT III SEGMENTATION OF GRAY LEVEL IMAGES 9

Histogram of gray level images, multilevel thresholding, Optimal thresholding using Bayesian classification, Watershed and Dam Construction algorithms for segmenting gray level image. Detection of edges and lines: First order and second order edge operators, multi-scale edge detection, Canny's edge detection algorithm, Hough transform for detecting lines and curves, edge linking.

UNIT IV IMAGE ENHANCEMENT AND COLOR IMAGE PROCESSING 9

Point processing, Spatial Filtering, Frequency domain filtering, multi-spectral image enhancement, image restoration. Color Representation, Laws of color matching, chromaticity diagram, color enhancement, color image segmentation, color edge detection, color demosaicing.

UNIT V IMAGE COMPRESSION 9

Lossy and lossless compression schemes, prediction based compression schemes, vector quantization, sub-band encoding schemes, JPEG compression standard, Fractal compression scheme, Wavelet compression scheme.

TOTAL : 45 PERIODS

OUTCOMES:

At the end of this course, the students should be able to:

- Discuss image enhancement techniques
- Explain color image processing
- Compare image compression schemes

REFERENCES:

1. A.K. Jain, "Fundamentals of Digital Image Processing", Prentice-Hall, Addison-Wesley, 1989.
2. Bovik (ed.), "Handbook of Image and Video Processing", Academic Press, 2000.
3. B. Jähne, "Practical Handbook on Image Processing for Scientific Applications", CRC Press,1997.
4. Bernd Jähne, Digital Image Processing, Springer-Verlag Berlin Heidelberg 2005.
5. Gonzalez and Woods, Digital Image Processing, Prentice-Hall.
6. J. C. Russ. The Image Processing Handbook. CRC, Boca Raton, FL, 4th edn., 2002.
7. J. S. Lim, "Two-dimensional Signal and Image Processing" Prentice-Hall, 1990.
8. M. Petrou, P. Bosdogianni, "Image Processing, The Fundamentals", Wiley, 1999.
9. Rudra Pratap, Getting Started With MATLAB 7. Oxford University Press, 2006
10. Stephane Marchand-Maillet, Yazid M. Sharaiha, Binary Digital Image Processing, A Discrete Approach, Academic Press, 2000
11. W. K. Pratt. Digital image processing, PIKS Inside. Wiley, New York, 3rd, edn., 2001.

VL5091 MEMS AND NEMS L T P C

3 0 0 3

OBJECTIVES:

- To introduce the concepts of microelectromechanical devices.
- To know the fabrication process of Microsystems.
- To know the design concepts of micro sensors and micro actuators.
- To familiarize concepts of quantum mechanics and nano systems.

UNIT I OVERVIEW 9

New trends in Engineering and Science: Micro and Nanoscale systems, Introduction to Design of MEMS and NEMS, MEMS and NEMS – Applications, Devices and structures. Materials for MEMS: Silicon, silicon compounds, polymers, metals.

UNIT II MEMS FABRICATION TECHNOLOGIES 9

Microsystem fabrication processes: Photolithography, Ion Implantation, Diffusion, Oxidation. Thin film depositions: LPCVD, Sputtering, Evaporation, Electroplating; Etching techniques: Dry and wet etching, electrochemical etching; Micromachining: Bulk Micromachining, Surface Micromachining, High Aspect- Ratio (LIGA and LIGA-like) Technology; Packaging: Microsystems packaging, Essential packaging technologies, Selection of packaging materials